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PATENT APPLICATION
2207/11270

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: FLETCHER, Thomas

Application No.: 09/956,903

Group Art Unit: 2816

Examiner: Not assigned

Filed: September 21, 2001

For: SYMMETRIC CASCADED DOMINO CARRY GENERATE CIRCUIT

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Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

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Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The paragraphs marked below are applicable.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date or the date of filing a CPA, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

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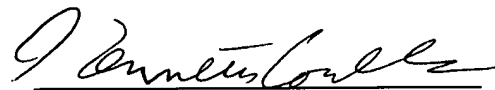
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Respectfully submitted,

KENYON & KENYON

Date: Feb 28, 2002



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Complete if Known

Application Number	09/956,903
Filing Date	September 21, 2001
First Named Inventor	FLETCHER, Thomas
Group Art Unit	2816
Examiner Name	Not assigned
Attorney Docket Number	2207/11270

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		6,208,907 B1	03/27/2002	DURHAM et al	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD- YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

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		Yee et al, "Clock-Delayed Domino for Dynamic Circuit Design", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 4, August 2000, pp 425-430	
		Yee et al, "Clock-Delayed Domino for Adder and Combinational Logic Design", IEEE, 1063-6404/96, pp 332-337, 1996	
		Jung, Perepelitsa, Sobelman, "Time Borrowing in High-Speed Functional Units Using Skew-Tolerant Domino Circuits," Proceedings, IEEE International Symposium on Circuits and Systems, pp. V-641 - V-644, 2000	
		Presentation by Carl Sechen dated March 17, 2000.	
		Taub, <i>Digital Circuits and Microprocessors</i> , pages 205-212, McGraw-Hill, 1982	

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